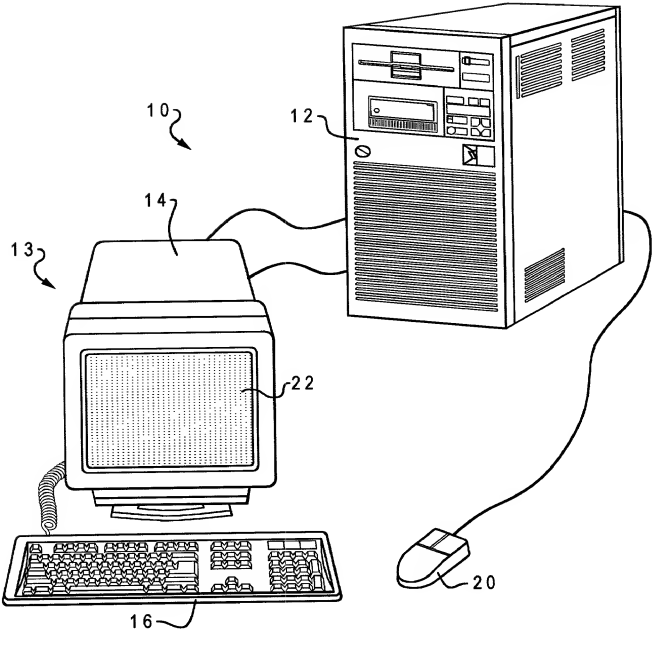

Fig. 1

10
CPU
24
ROM
30
RAM
28
DISK/TAPE DRIVE
33
I/O ADAPTER
34
COMMUNICATIONS ADAPTER
42
26
MAIN MEMORY
44
CONTROL PROGRAM
46
USER INTERFACE ADAPTER
36
DISPLAY ADAPTER
32
16
14
40
20
38

Fig. 2

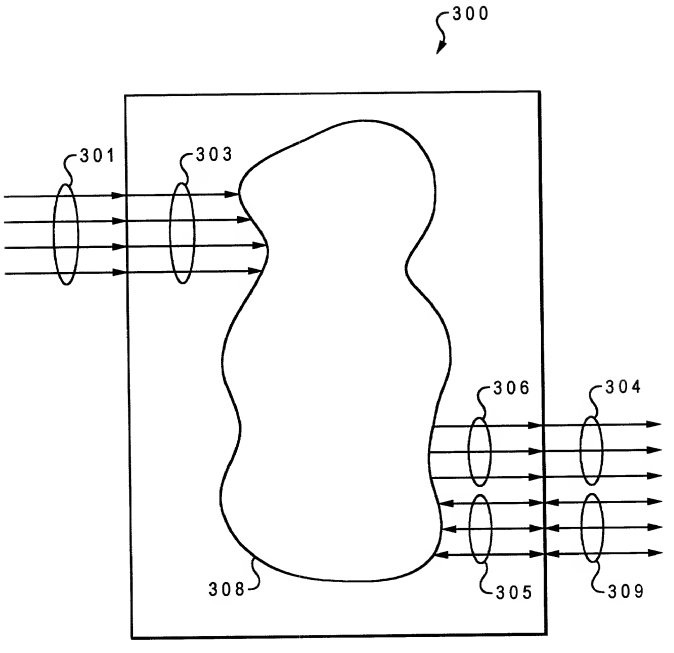

Fig. 3A

310
312
TOP:TOP
314
320
FXU:FXU0
A:A
B:B
C:C
325a
326a
327a
321a
FXU:FXU1
A:A
B:B
C:C
325b
326b
327b
321b
FPU:FPU0
322
329

Fig. 3B

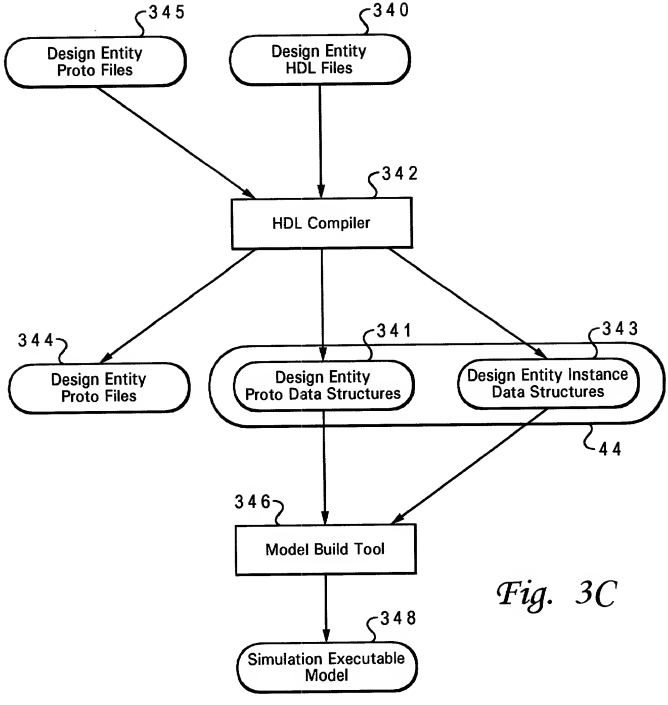
345
Design Entity Proto Files
340
Design Entity HDL Files
342
HDL Compiler
344
Design Entity Proto Files
341
Design Entity Proto Data Structures
343
Design Entity Instance Data Structures
44
346
Model Build Tool
348
Simulation Executable Model

Fig. 3C

Docket #AUS920000225US1

Fig. 3D

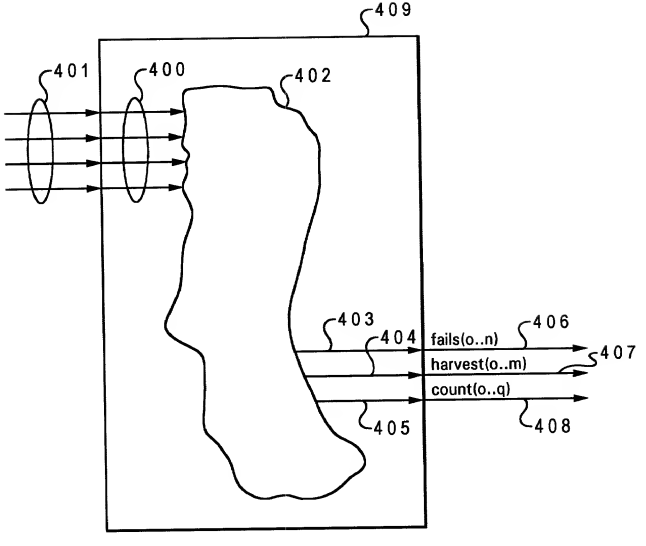
409
401
400
402
403
404
fails(o..n)
406
407
harvest(o..m)
count(o..q)
405
408

Fig. 4A

TOP:TOP
FXU:FXU0(a)
A:A
Q
372
B:B
C:C
S
374
FXUCHK
376
R
321b
325a
326a
327a
410
321a
415
FXU:FXU1(b)
A:A
Q
B:B
325b
C:C
S
326b
327b
FXUCHK
411
R
416
FPU:FPU0
FPUCHK
412
322
417
420
329
Counters
421
422
Harvest Flag
423
Fail
424

Fig. 4B

```
ENTITY FXUCHK IS

    PORT(   S_IN        :   IN std_ulogic;
            Q_IN        :   IN std_ulogic;
            R_IN        :   IN std_ulogic;
            clock       :   IN std_ulogic;
            fails       :   OUT std_ulogic_vector(0 to 1);
            counts      :   OUT std_ulogic_vector(0 to 2);
            harvests    :   OUT std_ulogic_vector(0 to 1);
        );

452 --!! BEGIN
    --!! Design Entity: FXU;

453 --!! Inputs
    --!! S_IN       =>      B.C.S;
    --!! Q_IN       =>      A.Q;
    --!! R_IN       =>      R;
    --!! CLOCK      =>      clock;
    --!! End Inputs

454 --!! Fail Outputs;
    --!! 0 : "Fail message for failure event 0";
    --!! 1 : "Fail message for failure event 1";
    --!! End Fail Outputs;

455 --!! Count Outputs;
    --!! 0 : <event0> clock;
    --!! 1 : <event1> clock;
    --!! 2 : <event2> clock;
    --!! End Count Outputs;

456 --!! Harvest Outputs;
    --!! 0 : "Message for harvest event 0";
    --!! 1 : "Message for harvest event 1";
    --!! End Harvest Outputs;

457 --!! End;

    ARCHITECTURE example of FXUCHK IS

    BEGIN

        ... HDL code for entity body section ...

    END;
```

450

451

458

440

Fig. 4C

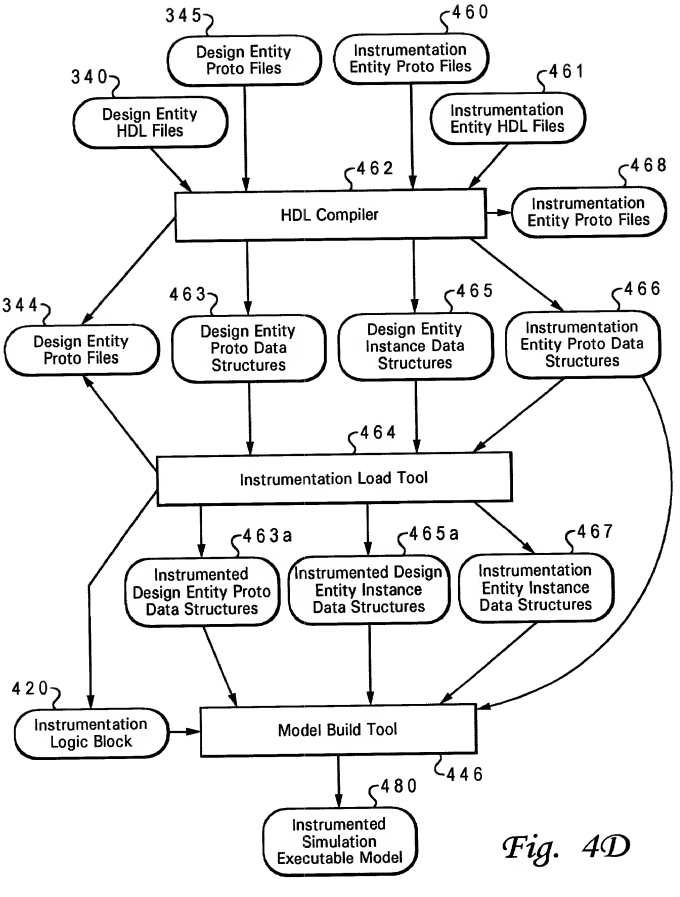
345
Design Entity Proto Files
460
Instrumentation Entity Proto Files
340
Design Entity HDL Files
461
Instrumentation Entity HDL Files
462
HDL Compiler
468
Instrumentation Entity Proto Files
344
Design Entity Proto Files
463
Design Entity Proto Data Structures
465
Design Entity Instance Data Structures
466
Instrumentation Entity Proto Data Structures
464
Instrumentation Load Tool
463a
Instrumented Design Entity Proto Data Structures
465a
Instrumented Design Entity Instance Data Structures
467
Instrumentation Entity Instance Data Structures
420
Instrumentation Logic Block
Model Build Tool
446
480
Instrumented Simulation Executable Model

Fig. 4D

FUCOMO 25225760

Fig. 4E

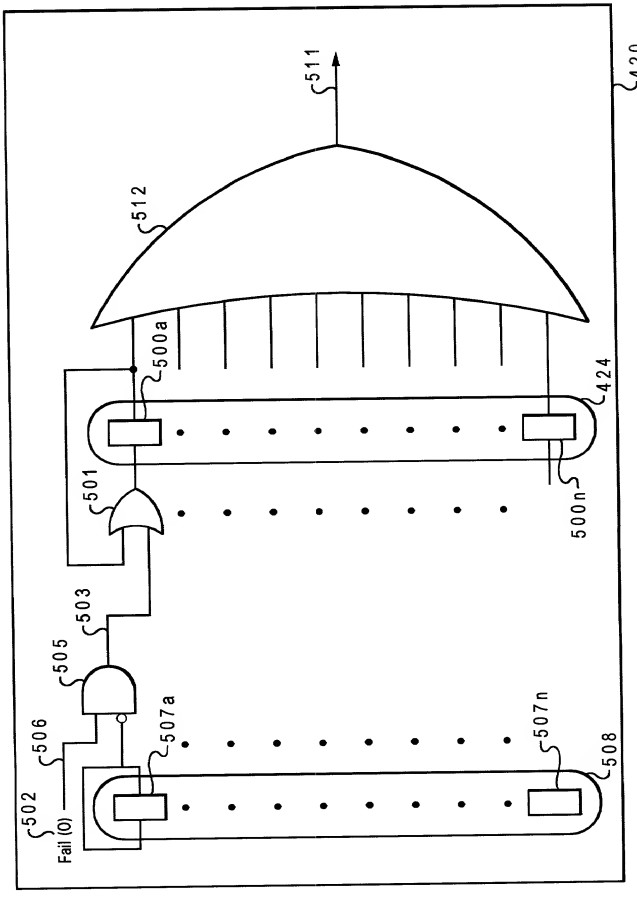
502
Fail (0)
506
505
503
501
507a
507n
508
500a
500n
424
512
511
420

Fig. 5A

Fig. 5B

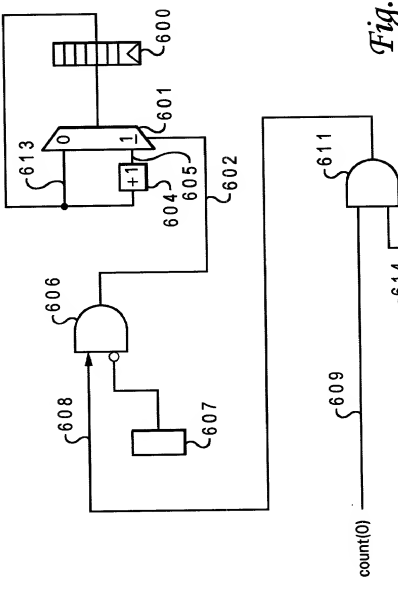
600
601
602
604
605
606
607
608
609
610
611
612
613
614
615
0
1
+1
count(0)
qualifier(0)

Fig. 6A

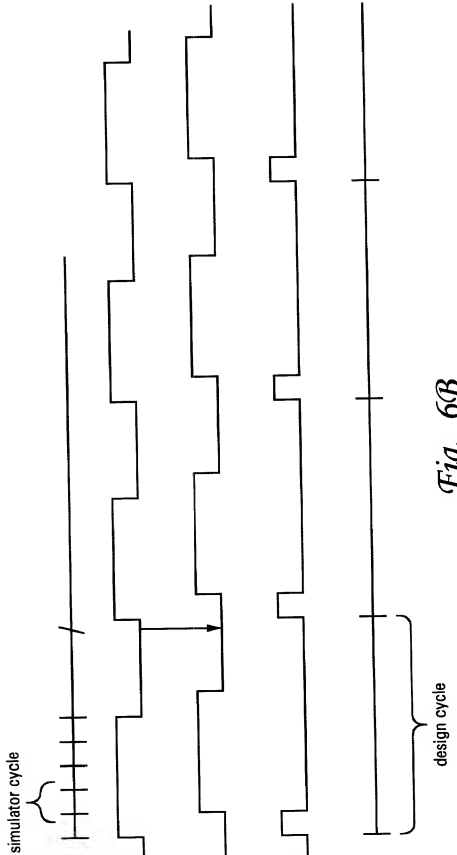

Fig. 6B

TUDOR 2002/60

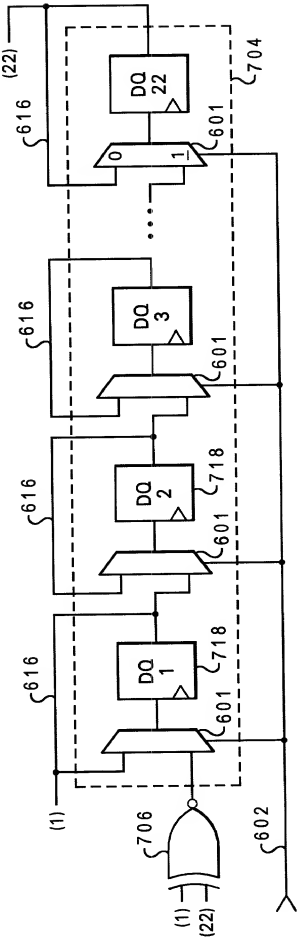

Fig. 7

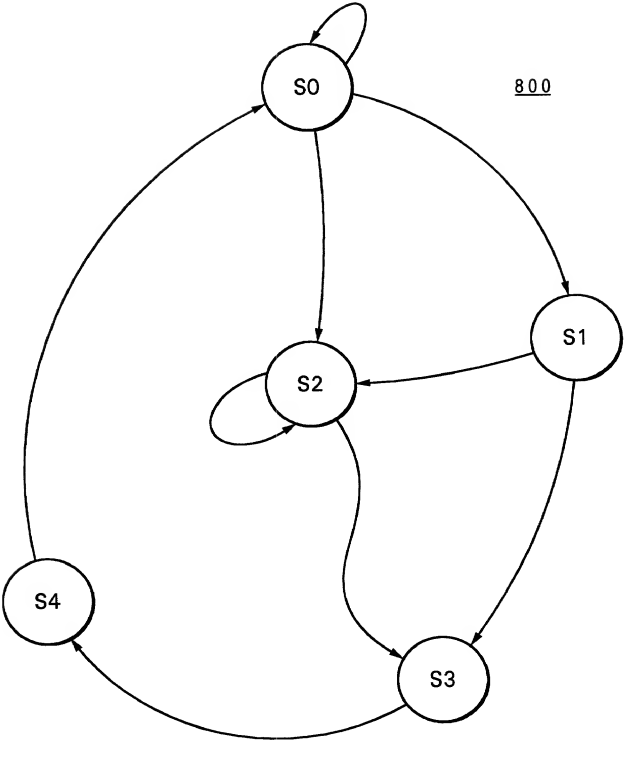

Fig. 8A
Prior Art

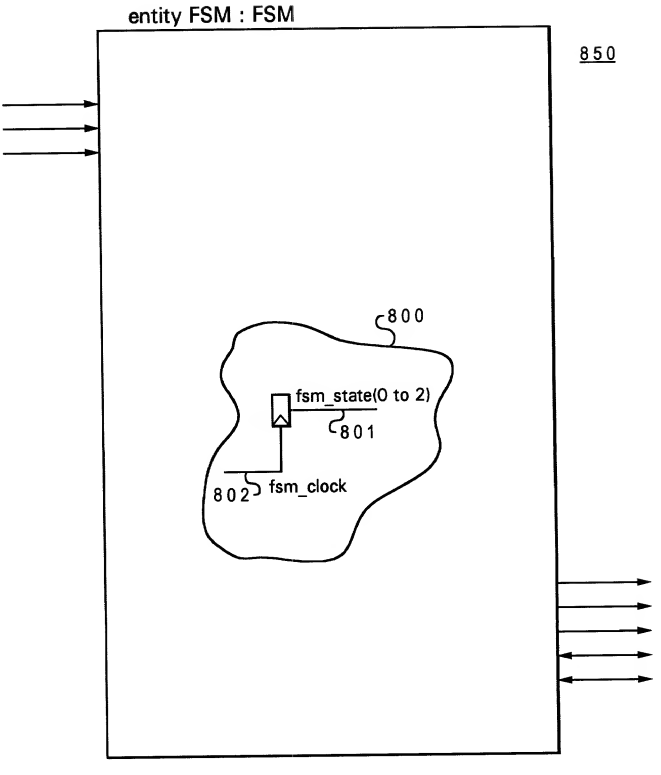

Fig. 8B
Prior Art

```
ENTITY FSM IS
    PORT(
            ....ports for entity fsm....
        );
    ARCHITECTURE FSM OF FSM IS
    BEGIN
            ... HDL code for FSM and rest of the entity ...
            fsm_state(0 to 2) < = ... Signal 801 ...
    853 --!! Embedded FSM : examplefsm;
    859 --!! clock        : (fsm_clock);
    854 --!! state_vector : (fsm_state(0 to 2));
    855 --!! states       : (S0, S1, S2, S3, S4);
    856 --!! state_encoding : ('000', '001', '010', '011', '100');
    857 --!! arcs         : (S0 = > S0, S0 = > S1, S0 = > S2,
        --!!               (S1 = > S2, S1 = > S3, S2 = > S2,
        --!!               (S2 = > S3, S3 = > S4, S4 = > S0);
    858 --!! End FSM;
                ,
                ,
                ,
                ,
                ,
                ,
                ,
    END;
```

852 860

Fig. 8C

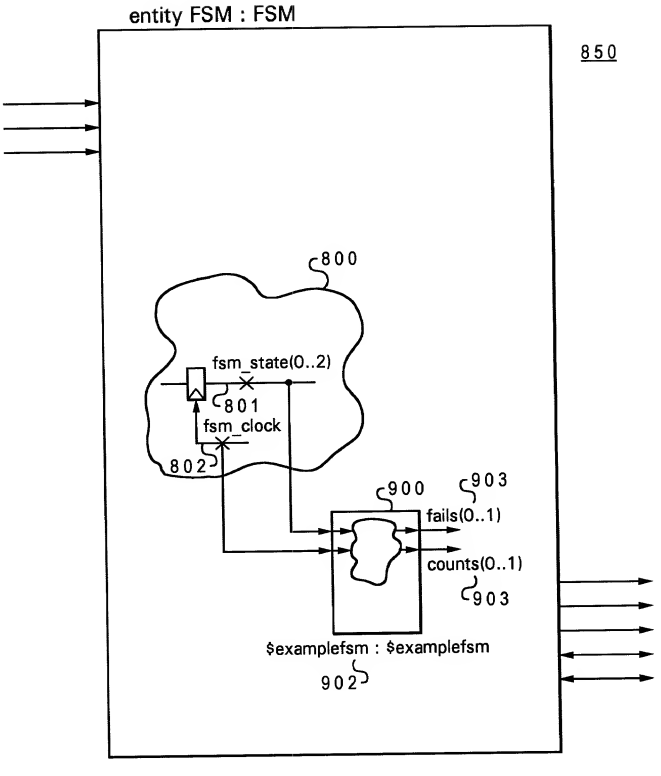
entity FSM : FSM
850
800
fsm_state(0..2)
801
fsm_clock
802
900
903
fails(0..1)
counts(0..1)
903
$examplefsm : $examplefsm
902

Fig. 9

Fig. 10A

09752252 - 040604

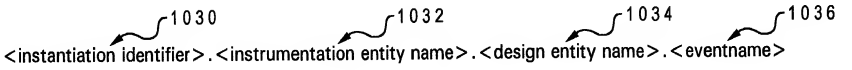

Fig. 10B

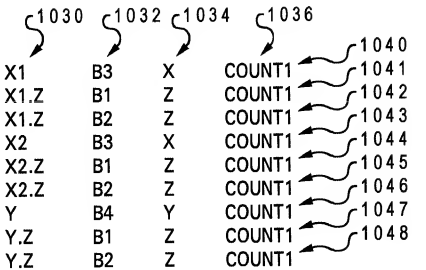

Fig. 10C

Fig. 10D

TOP:TOP
A:A
B:B
C:C
1102
1104
1106
1108
1110
1120
1122
1124
1126
1130
1132
1134
1150
1151
1152
1154
1156
B1:B1
B2:B2
B3:B3
event_1108_in
event_1124_in

Fig. 11A

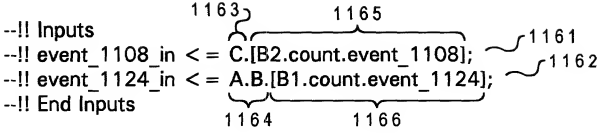

Fig. 11B

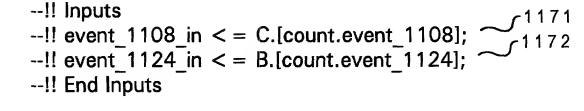

Fig. 11C

T06010.2522560

1200
X:X
1201
Y:Y
P
B1:B1
1202
1203
1208
1240
count
1241
fail
1242
harvest
Q
A
B
C

Fig. 12A

```
ENTITY X IS
     PORT(    :
              :
              :
         );
ARCHITECTURE example of X IS
BEGIN
      .
      .
      .
      .
      .
   ... HDL code for X ...
      .
      .
      .
      .
      .
   Y:Y
   PORT MAP(    :
                :
            );
   A <= ....
   B <= ....
   C <= ....
   --!! [count, countname0, clock] <= Y.P;
   --!! Q <= Y. [B1.count.count1] AND A;
   --!! [fail, failname0, "fail msg"] <= Q XOR B;
   --!! [harvest, harvestname0, "harvest msg"] <= B AND C;
END;
```

1220 1221 1222 1223 1230 1232 1234 1236

Fig. 12B

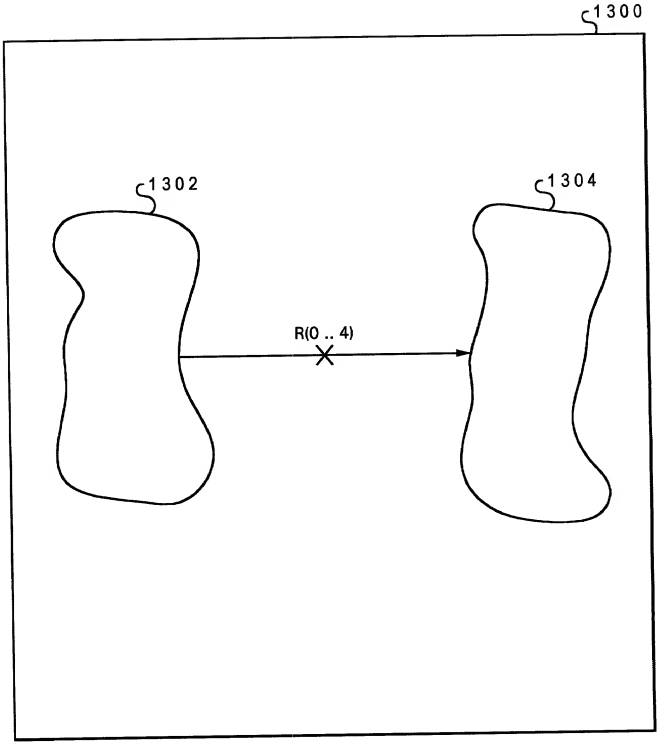

Fig. 13A

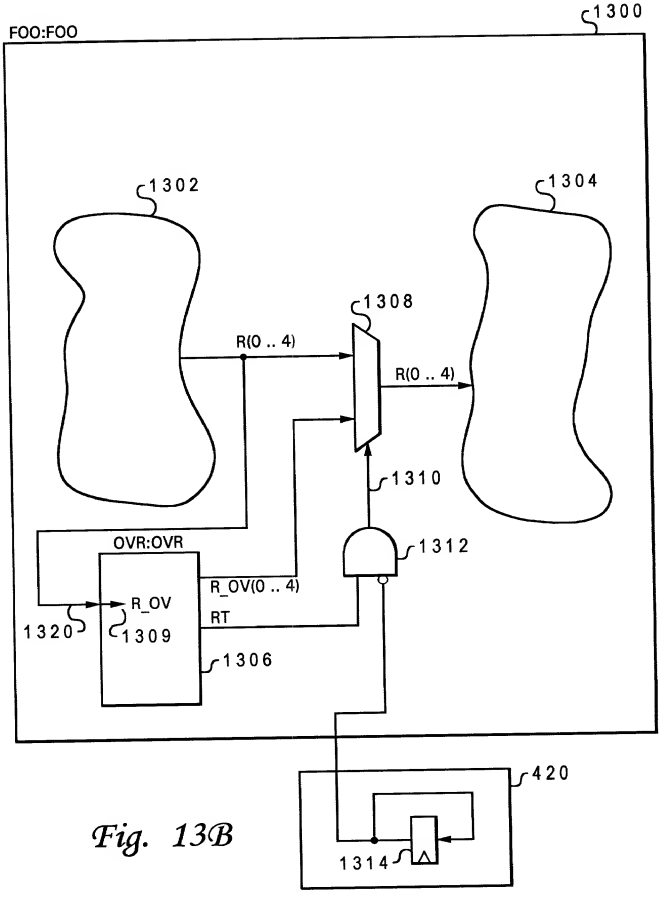
1300
FOO:FOO
1302
1304
1308
R(0 .. 4)
R(0 .. 4)
1310
1312
OVR:OVR
R_OV(0 .. 4)
R_OV
RT
1320
1309
1306
420
1314

Fig. 13B

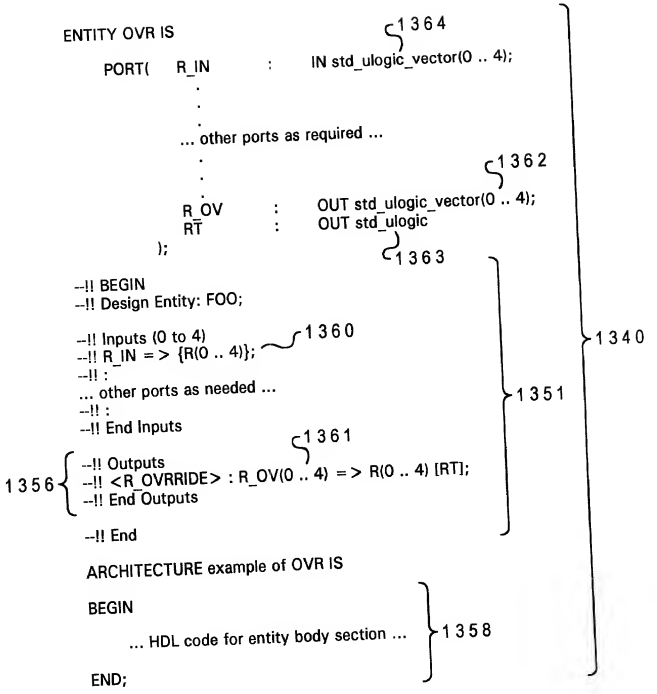
ENTITY OVR IS
1364
PORT(R_IN : IN std_ulogic_vector(0 .. 4);
... other ports as required ...
1362
R_OV : OUT std_ulogic_vector(0 .. 4);
RT : OUT std_ulogic
);
1363
--!! BEGIN
--!! Design Entity: FOO;
--!! Inputs (0 to 4)
--!! R_IN => {R(0 .. 4)};
1360
--!! :
... other ports as needed ...
--!! :
--!! End Inputs
1361
--!! Outputs
--!! <R_OVRRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];
--!! End Outputs
1356
--!! End
ARCHITECTURE example of OVR IS
BEGIN
... HDL code for entity body section ...
1358
END;
1351
1340

Fig. 13C

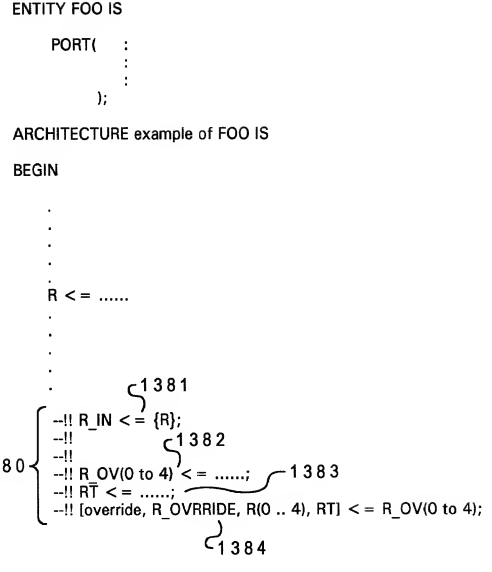
ENTITY FOO IS
PORT(:
:
:
);
ARCHITECTURE example of FOO IS
BEGIN
.
.
.
.
.
R <= .....
.
.
.
.
.
1381
--!! R_IN <= {R};
--!!
1382
--!!
1380
--!! R_OV(0 to 4) <= .....;
1383
--!! RT <= .....;
--!! [override, R_OVRRIDE, R(0 .. 4), RT] <= R_OV(0 to 4);
1384

Fig. 13D

44
1405
RTX
1430
GETFAC (A)
GETFAC (B)
GETFAC (C)
GETFAC (D)
1450
Processing Code
event_x = ...
1455
Simulator
1410
GETFAC
1400
LM:LM
A
P:P
C
Q:Q
B
D

Fig. 14A

1405
RTX
Simulator
1410
GETEVENT()
event_x =
GETEVENT()
1400
LM:LM
A
P:P
C
1462
1464
DET:DET
1466
1468
1460
Q:Q
B
D
1470
event_x .....

Fig. 14B

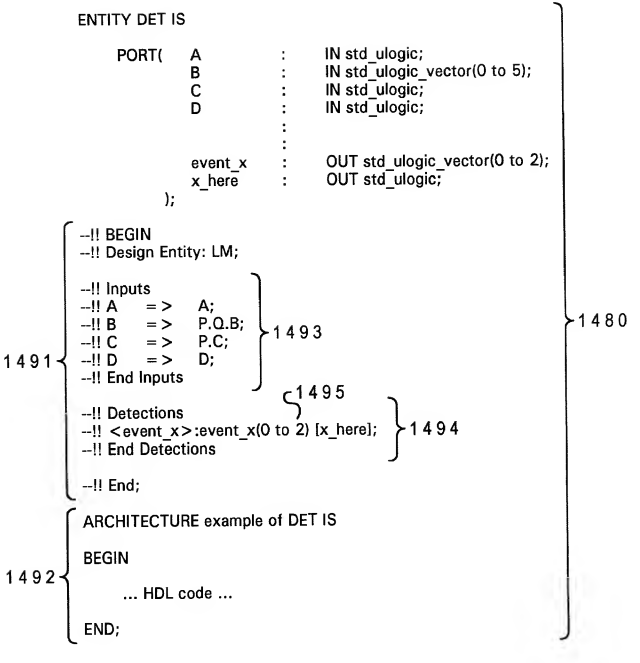
ENTITY DET IS
PORT(A : IN std_ulogic;
B : IN std_ulogic_vector(0 to 5);
C : IN std_ulogic;
D : IN std_ulogic;
event_x : OUT std_ulogic_vector(0 to 2);
x_here : OUT std_ulogic;
);
--!! BEGIN
--!! Design Entity: LM;
--!! Inputs
--!! A => A;
--!! B => P.Q.B;
--!! C => P.C;
--!! D => D;
--!! End Inputs
--!! Detections
--!! <event_x>:event_x(0 to 2) [x_here];
--!! End Detections
--!! End;
ARCHITECTURE example of DET IS
BEGIN
... HDL code ...
END;
1480
1491
1492
1493
1494
1495

Fig. 14C